

WHAT IS CLAIMED IS:

- 1 1. A method for manufacturing a semiconductor power device,
2 comprising:
 - 3 identifying an active region on a semiconductor die;
 - 4 identifying a first region in said active region;
 - 5 identifying a second region in said active region;
 - 6 providing a first cell design by which active cells in said first region will
7 be fabricated; and
 - 8 providing a second cell design by which active cells in said second region
9 will be fabricated,
 - 10 said first cell design being different from said second cell design.
- 1 2. The method of claim 1 wherein said first cell design and said
2 second cell design include cell dimensions such that a cell density of said first region is
3 different from that of said second region.
- 1 3. The method of claim 1 wherein said first cell design includes at
2 least one physical dimension different from that included in said second cell design.
- 1 4. The method of claim 3 wherein said physical dimension includes a
2 channel width.
- 1 5. The method of claim 4 wherein said physical dimension includes a
2 cell die area.
- 1 6. The method of claim 1 wherein said first cell design includes a
2 material composition for cells that is different from that of said second cell design.
- 1 7. The method of claim 1 wherein said first cell design differs from
2 said second cell design with respect to current density.
- 1 8. The method of claim 1 wherein said first cell design differs from
2 said second cell design with respect to source resistance.
- 1 9. The method of claim 1 wherein said first cell design differs from
2 said second cell design with respect to transconductance.

1 10. The method of claim 1 wherein said first cell design differs from
2 said second cell design with respect to gain.

1 11. The method of claim 1 wherein said first cell design differs from
2 said second cell design with respect to threshold voltage.

1 12. The method of claim 1 wherein said first cell design and said
2 second cell design are field effect transistors.

1 13. The method of claim 1 wherein said first cell design and said
2 second cell design are memory cells.